Self-Assessment problem 6-6

For the following set of events, show which routine the CPU is executing for times 0 to 100 nanoseconds (ns). Each handler routine (with its interrupt request) takes 20 ns to complete. The priority of the interrupts ranges from IRQ6 as the highest priority interrupt to IRQ1 as the lowest priority interrupt.

|  |  |
| --- | --- |
| **Time** | **Action** |
| 0 ns | start of main program |
| 10 ns | IRQ5 |
| 20 ns | IRQ3 |
| 45 ns | IRQ1 |
| 60 ns | IRQ4 |

**Answer**

|  |  |
| --- | --- |
| **Time (ns)** | **Routine** |
| 1 to 10 | main |
| 10 to 30 | IRQ5 |
| 30 to 50 | IRQ3 |
| 50 to 60 | IRQ1, because IRQ1 has to wait until 50 ns for the higher priority interrupt to complete |
| 60 to 80 | IRQ4, because IRQ4 is higher priority than IRQ1 at 60 ns |
| 80 to 90 | IRQ1 |
| 90 to 100 | main |